REMARKS

Present Status of the Application

Claims 1-4, 13 and 15 are pending of which claim 1 has been amended and claim 15 has been newly added. Amendment to claim 1 is fully supported at lines 5-14 of page 13. Therefore, it is believed that no new matter adds by way of amendment to claims or otherwise to the application.

In the Office Action dated December 21, 2004, the Examiner rejected claims 1 and 13 under 35 U.S.C. 103(a) as being unpatentable over Quigley et al. (US-5,781,388, hereinafter Quigley) in view of Jimenez et al. (US-5,646,433, hereinafter Jimenez); rejected claims 1, 3, 4 and 13 under 35 USC 103(a) as being unpatentable over Lin et al. (US-5,982,601, hereinafter Lin) in view of Jimenez; rejected claim 2 under 35 USC 103(a) as being unpatentable over Quigley and Jimenez or Lin and Jimenez in view of Ker et al. (US-5,754,380, hereinafter Ker). Applicants respectfully submit that at least for the following reasons claims 1-4, 13 and 15 patently define over prior arts of record. Reconsideration is respectfully requested.

Discussion of the claim rejection under 35 USC 103

1. The Office Action rejected claims 1 and 13 under 35 U.S.C. 103(a) as being unpatentable over Quigley et al. (US-5,781,388, hereinafter Quigley) in view of Jimenez et al. (US-5,646,433, hereinafter Jimenez).

In rejecting the above claims, the Examiner states that Quigley discloses, in FIG. 1, an ESD protection circuit similar to the claimed invention as claimed in claim 1 except for I/O pad not being directly connected to the voltage source and the anti-latch-up circuit. The Examiner further states that Jimenez, in FIG. 2 and 4 teaches a diode structure of protecting an I/O pad, such that the I/O pad is not directly connected to the voltage source and the anti-latch-up circuit. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a diode structure to protect the I/O pad in Quigley's device, such that the I/O pad is not directly connected to the voltage source and the anti-latch-up circuit in order to provide better protection to the device's components.

Applicants respectfully disagree and traverse the above rejections as set forth below.

The present invention is generally related to an ESD protection circuit. Particularly, claim 1, as amended, recites, among other things, "an anti-latch-up circuit, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal, respectively coupled to a voltage source, the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit is directly connected to the third connection terminal of the SCR circuit, [wherein a rising voltage rate at a

node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit] and thereby prevent latching up of the SCR circuit during normal operation".

The present inventors recognized that during the normal IC operation, in the event of an over-voltage, the voltage rising rate due to over-voltage is smaller that of the ESD pulse and accordingly designed the anti-latch-up circuit to determine the voltage rising rate to determine whether or not to trigger the SCR circuit and thereby prevent triggering of the SCR circuit due to over-voltage not caused by the ESD event. According to the claimed invention, when the voltage rising rate at the node of the anti-latch-up circuit is smaller than that of the ESD pulse, then it is determined to be normal IC operating condition and the latching up/triggering of the SCR circuit is prevented. On the other hand, when the voltage rising rate at the node of the anti-latch-up circuit is much faster than under the aforementioned normal IC operating condition, due to the ESD pulse, then it is determined to be abnormal IC operating condition, due to an ESD event, and the SCR circuit is triggered to bypass the ESD charge from the internal circuit to protect the internal circuit.

Instead, Quigley, at col. 4, lines 41-62, substantially discloses that a voltage, for example, 12 volts, is selected as trigger voltage at the pad, exceeding which the SCR circuit is triggered. Accordingly, Applicants respectfully submits that the voltage divider of Quigley is substantially designed to set a threshold voltage at the pad exceeding which the voltage divide generates an voltage to trigger the SCR circuit. In other words, Quigley substantially fails to teach or disclose a **[voltage rising rate at the node determines whether or not to trigger the SCR circuit]**,

instead, Quigley substantially teaches setting a threshold voltage at the pad to determine whether or not to generate a voltage to trigger the SCR circuit.

Furthermore, the proposed new claim 15 specify "a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse". In other words, because the RC delay time of the anti-latch up circuit is designed to be smaller than a voltage rising time of the IC power, therefore, the voltage at the node A change with the voltage source so that the voltage level at the node A is at the same level as that of the voltage source, and therefore the anti-latch-up circuit is capable of absorbing a large amount of carriers due to accidental over-voltage during the normal IC operation (not caused the ESD pulse) and thereby prevent latching up or triggering of the SCR circuit during the normal IC operation. On the other hand, during the ESD event, since the RC delay time of the anti-latch-up circuit is greater than the voltage rising time of the ESD pulse, the voltage level at the node A cannot out race the rising voltage at the pad due ESD pulse, thus the SCR circuit is activated to bypass the ESD charge from the internal circuit to protect the internal circuit.

Therefore, it is clear that the anti-latch-up circuit of the claimed invention does not generate any voltage to trigger the SCR circuit upon exceeding a threshold voltage at the pad as taught by Quigley, rather the anti-latch-up circuit is designed in manner discussed above so that a voltage rising rate at the node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit.

Accordingly, the anti-latch-up circuit is substantially different from the voltage divider (17, 18) of Quigley because the voltage divider is adopted to set up a threshold voltage exceeding which a voltage is generated in order to trigger the SCR circuit whereas the anti-latch-up circuit of the present invention is adopted to determine the voltage rising rate at the node to determine whether or not to trigger the SCR circuit.

Furthermore, Applicants would like to point out that Jimenez, at line 21 of col. 1 to line 7 of col. 2, FIGS. 1 and 2, substantially discloses a CONVENTIONAL pad protection diode structure, wherein a pad is connected to the input gate of a MOS transistor. The integrated circuit is coupled between a high supply voltage VDD and a low supply voltage VSS, for example, ground. The pad is connected to the low and high voltage terminals through biased diodes D1 and D2, as shown in FIG. 1. However, Jimenez fails to even mention either an anti-latch-up circuit or a voltage divider. Accordingly, Applicants respectfully submit that even when Quigley and Jimenez were combined in a manner suggested by the Examiner, still the combination cannot possibly achieve every features of the claimed invention as claimed in claim 1 in this regard.

Therefore, Quigley and Jimenez substantially fail to teach, suggest or hint every features of Claim 1, and therefore cannot render every features of Claim 1.

Claim 13, which directly depends from Claim 1, is also patentable over Quigley, at least because of their dependency from an allowable base claim. Reconsideration is respectfully requested.

For at least the foregoing reasons, claims 1, 13 and 15 patently define over Quigley and Jimenez. Reconsideration and withdrawal of the above rejections is respectfully requested.

2. The Office Action rejected claims 1, 3, 4 and 13 under 35 USC 103(a) as being unpatenble over Lin et al. (US-5,982,601, hereinafter Lin) in view of Jimenez.

Applicants respectfully disagree and would like to point out that, Lin substantially shows that the transient generator (51) is adapted to provide a voltage transition such that the P+/n well junction of the SCR is forward biased a number of times during early stage of an ESD event. Furthermore, Lin substantially teaches that the transient generator (51) is comprised of an oscillator circuit (61) and the oscillator circuit (61) which is adopted to generate fast clocks during the early stage of the ESD transient to trigger the SCR circuit. Accordingly, the transient generator/oscillator circuit (51, 61) of Lin is substantially different from the anti-latch-up circuit of the claimed invention because the transient generator/oscillator circuit (51, 61) of Lin is adopted to generate fast clocks during the early stage of the ESD transient to trigger the SCR circuit whereas the anti-latch-up circuit of the present invention is adopted to determine the voltage rising rate at the node to determine whether or not to trigger the SCR circuit.

Accordingly, Applicants respectfully submit that even when Lin and Jimenez were combined in a manner suggested by the Examiner, still the combination cannot possibly achieve every features of the claimed invention as claimed in claim 1 in this regard.

Claims 3, 13, and 15, which directly depend from Claim 1 is also patentable over Lin and Jimenez, at least because of their dependency from an allowable base claim. Reconsideration is respectfully requested.

3. The Office Action rejected claim 2 under 35 USC 103(a) as being unpatenble over Quigley and Jimenez or Lin and Jimenez in view of Ker et al. (US-5,754,380, hereinafter Ker).

Applicants respectfully disagree and would like to point out that even though the Examiner relied upon Ker or Jimenez to disclose a first diode and a second diode, still Ker or Jimenez cannot cure the specific deficiencies of Quigley or Lin as discussed above with respect to independent claim 1. Reconsideration and withdrawal of the above rejection is respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-4, 13 and 15 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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